Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A data processing device, comprising:

~~a master controller,~~

a first functional unit <u>for performing one or more operations having a relatively long latency, the first functional unit</u> including a slave controller,

a second functional unit <u>for performing one or more operations having a relatively short latency</u>, ~~and~~

a common memory means shared by the first and second functional units, <u>and</u>

~~the data processing device being programmed~~ <u>a master controller for controlling a schedule</u> for executing an instruction by the first functional unit, <u>the</u> execution of said instruction ~~involving~~ <u>including</u> input/output operations <u>that are performed</u> by <u>the slave controller of</u> the first functional unit,

wherein said ~~execution involves~~ <u>master controller synchronizes</u> at least one of~~:~~ output data of the first functional unit ~~being~~ processed by the second functional unit during <u>the</u> execution of said instruction~~,~~ and the input data to the first functional unit being generated by the second functional unit during <u>the</u> execution of said instruction.

2. (Canceled)

3. (Currently amended) The data processing device according to claim 1, ~~having~~ further

comprising halt means controllable by the master controller for suspending operation of the

first functional unit.

4. (Currently amended) A method of operating a data processing device, comprising:

~~a master controller for controlling operation of the data processing device,~~

a first functional unit, which includes a slave controller, the first functional unit being

arranged for executing ~~instructions of a first type corresponding to~~ operations having a

relatively long latency,

a second functional unit capable of executing ~~instructions of a second type~~

~~corresponding to~~ operations having a relatively short latency, and

~~wherein the first functional unit~~ a master controller to control a schedule for

executing an instruction by the slave controller, during execution of ~~an~~ the instruction ~~of the~~

~~first type~~ the first functional unit receives input data and provides output data, and

wherein said ~~execution involves~~ master controller synchronizes at least one of~~:~~ output data

of the first functional unit ~~being~~ processed by the second functional unit during the

execution of said instruction~~,~~ and the input data to the first functional unit being generated

by the second functional unit during the execution of said instruction.

5. (Currently amended) The method according to claim 4, ~~wherein~~ further comprising an act of the master controller temporarily ~~suspends~~ suspending operation of the first functional unit during execution of ~~instructions of the first type~~ the instruction.